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Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS — SECTIONAL SPECIFICATION FOR FILM INTEGRATED CIRCUITS AND HYBRID FILM INTEGRATED CIRCUITS ON THE BASIS OF QUALIFICATION APPROVAL PROCEDURE

ICS 31.200

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BUREAU OF INDIAN STANDARDS
MANAK BHAVAN, 9 BAHADUR SHAH ZAFAR MARG
NEW DELHI 110002

January 1996

Price Rs 80.00

Semiconductor Devices and Integrated Circuits Sectional Committee, LT 10

NATIONAL FOREWORD

This Indian Standard, which is identical with IEC Pub 748-21/QC 760100 (1991) 'Semiconductor devices — Integrated circuits — Part 21 : Sectional specification for film integrated circuits and hybrid film integrated circuits on the basis of qualification approval procedure', issued by the International Electrotechnical Commission (IEC), was adopted by the Bureau of Indian Standards on the recommendation of Semiconductor Devices and Integrated Circuits Sectional Committee (LT 10) and approval of the Electronics and Telecommunication Division Council.

The text of the IEC standard has been approved as suitable for publication as Indian Standard without deviations. Certain conventions are, however, not identical to those used in Indian Standards. Attention is particularly drawn to the following :

a) Wherever the words 'International Standard' appear referring to this standard, they should be read as 'Indian Standard'.

b) Comma (,) has been used as a decimal marker while in Indian Standards, the current practice is to use a point (.) as the decimal marker.

In the adopted standard, reference appears to certain International Standards for which Indian Standards also exist. The corresponding Indian Standards which are to be substituted in their place are listed below along with their degree of equivalence for the editions indicated :

International Standard	*Corresponding Indian Standard*	*Degree of Equivalence*
IEC Pub 748-20/QC 760000 (1988) Semiconductor devices — Integrated circuits — Part 10 : Generic specification for film integrated circuits and hybrid film integrated circuits	IS QC 760000 (1994) Semiconductor devices — Integrated circuits : Generic specification for film integrated circuits and hybrid film integrated circuits	Identical

The concerned technical committee has reviewed the provisions of the IEC Pub 63 (1963), Amendment 1 (1967) and Amendment 2 (1977), referred in this adopted standard and has decided that they are acceptable for use in conjunction with this standard.

This standard is intended primarily for use under the IECQ System. A regular Indian Standard for this component could be different, identical or similar to this standard.

Only the English language text in the International Standard has been retained while adopting it in this Indian Standard.

IS QC 760100 (1995)
IEC QC 760100 (1991)

Indian Standard

SEMICONDUCTOR DEVICES — INTEGRATED CIRCUITS — SECTIONAL SPECIFICATION FOR FILM INTEGRATED CIRCUITS AND HYBRID FILM INTEGRATED CIRCUITS ON THE BASIS OF QUALIFICATION APPROVAL PROCEDURE

1 Scope and object

1.1 *Scope*

This sectional specification applies to film integrated circuits and hybrid film integrated circuits, manufactured as catalogue products or as custom-built products whose quality is assessed on the basis of Qualification Approval.

1.2 *Object*

The object of this specification is to present preferred values for ratings and characteristics, to select from the generic specification the appropriate tests and measuring methods and to give general performance requirements to be used in detail specifications for film integrated circuits and hybrid film integrated circuits derived from this specification.

Test severities and requirements prescribed in detail specifications referring to this sectional specification shall be of equal or higher performance level, because lower performance levels are not permitted.

Associated with this specification are one or more blank detail specifications, each referenced by an IEC number. A blank detail specification which has been completed as specified in subclause 2.3 of this specification forms a detail specification. Such detail specifications shall be used for the granting of Qualification Approval to a film integrated circuit or hybrid film integrated circuit and Quality Conformance Inspection in accordance with the IECQ system.

2 General preferred characteristics, ratings and severities for environmental tests

2.1 *Related documents*

Publication 63 (1963):	Preferred number series for resistors and capacitors. Amendment 1 (1967). Amendment 2 (1977).
Publication 748-20 (1988):	Semiconductor devices - Integrated circuits, Part 20: Generic specification for film integrated circuits and hybrid film integrated circuits.

2.2 *Preferred ratings and characteristics*

Preferred values of voltages and currents are given in IEC Publication 747-1; for resistors and capacitors preferred values are given in IEC Publication 63; for custom-built circuits, any values and tolerances may be chosen.

2.3 *Information to be given in a detail specification*

Detail specifications shall be derived from the relevant blank detail specification.

Detail specifications shall not specify severities inferior to those of the Generic or Sectional specification. When more severe requirements are included, they shall be listed in the detail specification and indicated in the test schedules, for example by an asterisk.

NOTE - The information given on dimensions, characteristics and ratings may, for convenience, be presented in tabular form.

The following information shall be given in each detail specification and the values quoted shall preferably be selected from those given in the appropriate clause of this sectional specification.

Each detail specification shall prescribe all the tests and measurements required for lot-by-lot inspection and periodic testing. It shall, as a minimum, include the relevant tests given in this specification with methods and severities.

2.3.1 *Outline drawing and dimensions*

There shall be an illustration of the circuit as an aid to easy recognition and for comparison of the circuit with others. Dimensions and their associated tolerances, which affect interchangeability and mounting, shall be prescribed in the detail specification. All dimensions shall be stated in millimetres.

Normally, numerical values shall be given for the length, the width and height of the body, and the termination spacing or, for cylindrical types, the body diameter and the length and diameter of the terminations.

When necessary, for example when in a detail specification more than one package is covered, the dimensions and their associated tolerances shall be placed in a table below the drawing.

When the configuration is other than that described above, the detail specification shall state such dimensional information as to adequately describe the circuit.

2.3.2 *Mounting*

The detail specification shall prescribe the method of mounting to be applied for normal use and for the application of the mechanical tests. The design of the circuits may be such that special mounting fixtures are required in its use. In this case, the detail specification shall prescribe the mounting fixtures and they shall be used in the application of the mechanical tests.

2.3.3 *Severities for environmental tests*

The detail specification shall prescribe the appropriate method of testing and the appropriate severities selected from section 4 of the generic specification.

2.3.4 *Marking*

The detail specification shall prescribe the content of the marking on the circuit and on the primary package. Deviations from subclause 2.6 of the generic specification shall be specifically stated.

2.3.5 *Ordering information*

The detail specification shall prescribe that the following information is required when ordering circuits.

1) circuit type (for example, hybrid thick film integrated circuit);
2) number of the detail specification with type reference and assessment level (if appropriate);
3) function of the circuit (if appropriate);
4) basic functional characteristics with tolerance (if appropriate).

2.3.6 *Additional information* (not for inspection purposes)

The detail specification may include information which is not normally required to be verified by the inspection procedure, such as circuit diagrams, curves, drawings and notes needed for clarification.

3 Qualification approval procedures

See subclause 3.5 of the Generic Specification with the following details:

3.1 *Structural similarity*

For the purpose of assessment testing, structural similarity can be used if the testing of one representative type of circuit gives at least the same quality for the rest of the types which are grouped together.

The Chief Inspector shall declare, to the satisfaction of the NSI, the method of operating the structural similarity plan within the manufacturing facilities and the representative type(s) from each structurally similar group.

For the qualification approval procedure, two or more circuits can be considered structurally similar, and thus the required numbers of specimens for a test shall be selected from the combined production, when they have the same function type, use the same design rules, materials, processes and methods (for example, a range of T-cell thick-film attenuators using the same line of inks; or thin-film D/A convertors using the same film material and same film material and same added components from the same supplier).

For visual examination, marking, dimensions, sealing, solderability, robustness of terminations, the only requirement is an identical envelope. Empty packages and/or electrical rejects may be used.

3.2 *Qualification approval*

The procedures for Qualification Approval testing are given in subclause 3.5 of the generic specification.

The schedules to be used for qualification approval testing on the basis of lot-by-lot and periodic testing are given in tables 2 and 3 of the blank detail specification.

The procedure for qualification approval on the basis of the fixed sample size schedule is given in table 1.

The tables for qualification approval (fixed sample size schedule) and quality conformance inspection (lot-by-lot and periodic tests) collectively prescribe the minimum test programme on completed circuits.

The manufacturer may select which assessment level K, L or M he wishes to adopt, but may release products only as follows:

Assessment level	*Release assessment level*
K	K, L or M
L	L or M
M	M

A manufacturer may change the assessment level of his approval by completing the relevant tests. Subject to NSI agreement, he may downgrade without further periodic testing until current test interval dates expire.

Any additional tests required for specific applications shall be prescribed in the detail specification.

The post-test electrical limits for the relevant environmental tests shall be prescribed in the detail specification.

3.2.1 *Qualification approval* (fixed sample size procedure)

3.2.1.1 *Sampling*

The sample shall be representative of the range of circuits for which approval is required. The size of the sample and the criterion of acceptability depend on the assessment level which is claimed and are detailed in table 2.

When additional groups are introduced into the test schedule, the number of circuits required for Group "0" shall be increased by the same number as that required for the additional groups.

3.2.1.2 *Tests*

The complete series of tests specified in table 1 is required for the approval of circuits covered by one detail specification. The tests in each group shall be carried out in the given order.

The whole sample shall be subjected to the tests of Group "0" and then divided for the other groups.

Circuits found defective during the tests of Group "0" shall not be used for the other groups.

"One defective device" is counted when a circuit has not complied with the whole or a part of the tests of a group.

The approval is granted when the number of defective devices does not exceed the specified number of permissible defective devices for each group or sub-group and the total number of permissible defective devices.

Table 1 - Test schedule for qualification approval procedure

Sample sizes and acceptance criteria are detailed for each assessment level in table 2.

NOTE - Subclause numbers refer to section 4 of the generic specification.

Clause numbers, tests and test sequences	D or ND	Test conditions	Inspection requirements
Group 0 *Sub-group 01* 4.3.1 Precap visual examination	ND		
Sub-group 02a 4.3.2 External visual examination and marking	ND		
Sub-group 02b 4.3.3 Dimensions	ND		
Sub-group 03 (Note 7) 4.5.16 Induced flammability (for information only)	D		
Sub-group 04 (Note 1) 4.5.9 Sealing	ND		
Sub-group 05 4.4.11 Major static and dynamic electrical characteristics at room temperature	ND		
Sub-group 06 4.4.11 Major static and dynamic electrical characteristics at extreme operating temperatures	ND		
Group 1 Sequence (Note 1) (Note 2)			
Initial measurements	D/ND	4.4.11: Sub-group 05	
4.5.6 Vibrations, swept frequency and 4.5.7 Acceleration, steady state or (Note 3) 4.5.5 Shocks and 4.5.7 Acceleration, steady state			
Final measurements		4.5.9: Sealing 4.4.11: Sub-group 05	

For notes, see page 7.

Table 1 (*continued*)

Clause numbers, tests and test sequences	D or ND	Test conditions	Inspection requirements
Group 2	D		
Initial measurements		4.4.11: Sub-group 05	
4.5.11 Resistance to soldering heat			
4.5.15.2 Resistance to solvents (Note 7)			
4.5.8 Change of temperature			
4.5.3 Damp heat, steady state (Note 4)			
Final measurements		4.5.9: Sealing (Note 1)	
		4.4.11: Sub-group 05	
		4.3.2: External visual examination and marking	
Group 3 (Note 5)	D		
4.5.10 Solderability			
4.5.12 (Note 1) Tensile			
(Note 3) Bending (wire or strip)			
Final measurements		4.5.9: Sealing (Note 1)	
or (Note 3)			
4.5.10 Solderability			
4.5.12 (Note 1) Tensile			
(Note 3) Bending (row)			
(Note 2) Thrust			
Final measurements		4.5.9: Sealing (Note 1)	
Group 4	ND		
Initial measurements		4.4.11: Sub-group 05	
4.5.2 Cold		Temperature: ..... °C	
4.5.1 Storage at high temperature		Temperature: ..... °C	
Final measurements		4.4.11: Sub-group 05	
Group 5	D		
Initial measurements		4.4.11: Sub-group 05	
4.5.14 Endurance: 1 000 h			
Endurance: 2 000 h (Note 6)			
Final measurements		4.4.11: Sub-group 05	

NOTES

1 Cavity circuits only.

2 Mounting conditions as prescribed by the detail specification.

3 The detail specification shall prescribe which option is to be used.

4 The detail specification may omit the damp heat test for encapsulated circuits.

5 Use of completely processed electrical rejects is permitted.

6 In assessment level K: provisional approval after 1 000 h;
definitive approval after 2 000 h.

7 Applicable to circuits having organic material used for encapsulation.

3.2.2 *Quality conformance inspection*

3.2.2.1 *Formation of inspection lots*

An inspection lot shall consist of structurally similar circuits (see subclause 3.1).

Screening (if required) applies to all circuits intended for release to customers.

For A and B tests, the sample shall be collected from one week's production, or such other period as declared by the manufacturer up to a maximum of one month.

3.2.2.2 *Tests*

The test schedules for the lot-by-lot and the periodic tests are prescribed in the relevant blank detail specification.

The complete series of tests specified are required for the maintenance of the qualification approval of circuits covered by one detail specification.

The tests in each group shall be carried out in the order given.

"One defective device" is counted when a circuit has not complied with the whole or a part of the tests of a group.

The approval is maintained when the number of defective devices does not exceed the specified number of permissible defective devices for each group and the total number of permissible defective devices.

3.3 *Assessment levels*

The assessment level(s) for qualification approval shall be selected from table 2 below. (For the test schedule, see table 1.)

The assessment level(s) for quality conformance inspection (see relevant blank detail specification) shall be selected from table 3.

Table 2 - Assessment levels and acceptance criteria for qualification approval

In this table:

n = sample size

c = acceptance criterion (permissible number of defective devices).

Inspection group or sub-group of table 1	Assessment level								
	K			L			M		
	n	c		n	c		n	c	
01	100 %	(Note 3)		-	-		-	-	
02a	75 (Note 1)	2		64 (Note 1)	2		43	2	
02b	8	1		8	1		8	1	
03 (for information only)	2	-		2	-		2	-	
04	39	1	2	26	1	2	13	1	2
05	71 (Note 1)	1		60 (Note 1)	1		39	1	
06	26	1		13	1		8	1	
1	10	1	2	8	1	2	-	-	2
2 (Note 2)	13	1		10	1		8	1	
3	13	1		10	1		8	1	
4	13	1		10	1		8	1	
5 (1 000 h)	-	-		20	1		13	1	
(2 000 h)	20	1		-	-		-	-	

NOTES

1 This number may be reduced by the relevant number of circuits which are not needed when the test in Group 1 is not required.

2 A minimum of four circuits shall be used for each solvent specified.

3 According to the detail specification.

Table 3 - Assessment levels and acceptance criteria for quality conformance inspection

Table 3A - Lot-by-lot tests to be conducted on a sampling basis

In this table:

IL = inspection level.

AQL = acceptable quality level.

Clause numbers refer to section 4 of the generic specification.

Inspection group or sub-group	**Assessment level**					
	K		L		M	
Screening (see table 4)	Required		Not required		Not required	
	IL	AQL	IL	AQL	IL	AQL
Sub-group A1 4.3.2 External visual examination and marking	II	1	II	2,5	I	2,5
Sub-group A2 4.4.11 Major static and dynamic electrical characteristics at room temperature	II	0,25	II	0,4	II	1
Sub-group A3 4.4.11 Major static and dynamic electrical characteristics at extreme operating temperatures	S4	1	-	-	-	-
Sub-group B1 4.5.10 Solderability	S3	2,5	S3	2,5	S3	2,5
Sub-group B2 4.3.3 Dimensions	S4	1	S4	1	S4	1

Table 3B - Periodic tests to be conducted on a sampling basis

In this table:

p = periodicity (in months)

n = sample size

c = acceptance criterion (permissible number of defective devices).

Clause numbers refer to section 4 of the generic specification.

Inspection group or sub-group	Assessment level											
	K				L				M			
	p	n	c		p	n	c		p	n	c	
Sub-group C1 4.4.11 Major static and dynamic electrical characteristics at extreme temperatures	6	20	1		6	13	1		6	8	1	
Sub-group C2 Sequence (Note 1) (Note 2) 4.5.6 Vibration, swept frequency and 4.5.7 Acceleration, steady state or (Note 3) 4.5.5 Shock and 4.5.7 Acceleration, steady state	6	10	1	2	12	8	1	2	-	-	-	2
Sub-group C3 Sequence 4.5.11 Resistance to soldering heat 4.4.15.2 Resistance to solvents (Note 7) 4.5.8 Change of temperature 4.5.3 Damp heat, steady state (Note 4)	6	13	1		12	10	1		12	8	1	
Sub-group C4 Sequence 4.5.2 Cold 4.5.1 Storage at high temperature	6	13	1		12	12	1		12	8	1	
Sub-group D1 4.5.14 Endurance: 1 000 h	-	-	-		6	20	1		6	13	1	
Endurance: 2 000 h (Note 6)	6	20	1		-	-	-		-	-	-	
Sub-group D2 Sequence (Note 5) 4.5.12 (Note 1) Tensile (Note 3) Bending (wire or strip) or (Note 3) (Note 1) Tensile (Note 3) Bending (row) (Note 2) Thrust	12	13	1		12	10	1		12	8	1	
4.5.16 Induced flammability (Note 7) (for information only)	12	2	-		12	2	-		12	2	-	

For notes see page 7.

Screening

Sequences for screening shall be in accordance with the following table 4.

Table 4 - Screening

Steps	Examination or test	Generic specification reference	Details and conditions	Sequences				
				A	B	C	D	E
1*	Precap visual inspection	4.3.1	Under consideration	x				
2	Storage at high temperature	4.5.1	24 h at max. storage temperature	x	x	x		x
3	Change of temperature	4.5.8	10 cycles T_{stg} min. / T_{stg} max.	x	x	x		x
4*	Constant acceleration	4.5.7	*In the most critical direction. Acceleration level as specified in the detail specification*	x	x	x		
5*	Sealing	4.5.9		x	x	x		
6	Electrical measurements (pre burn-in)		Selected parameters Remove defective devices	x 1)	x		x	
7	Burn-in		As specified in the detail specification hours:	x 168	x 72		x 48	
8	Electrical measurements (post screening)		As specified in 6. Remove defective devices Remove lot if defects exceed 10 %	x	x	x	x	x

* Normally not applicable to non-cavity devices, unless otherwise indicated in the detail specification.

1) Record the results of the measurements unless otherwise specified in the detail specification.

NOTE - Screening is normally performed before Group A, B and C inspection. When screening is performed after meeting the requirements of Groups A and B on a lot-by-lot basis and Group C on a periodic basis, the solderability, sealing and Group A tests shall be repeated.

Additional post-screening tests may be required as specified in the blank detail specification.

3.4 *Resubmission of rejected lots (lot-by-lot inspection)*

Any lot rejected following electrical tests shall be returned to production for rework or rescreening for the identified defect. No new circuit shall be included in the lot.

The lot shall then be resubmitted and inspected under conditions of tightened inspection.

The same lot number is retained and details of the new submission will be recorded. The same lot shall not be submitted more than three times.

3.5 *Manufacturing stages in a factory of an approved manufacturer in a non-IEC member country*

The application of the extension of manufacturer's approval is permitted for the film integrated circuits and hybrid film integrated circuits covered by this specification, provided that the conditions of subclause 3.2 of the generic specification are met.

4 Test and measurement procedures

This clause contains all tests and measurement procedures which are of typical application for film integrated circuits and hybrid film integrated circuits and which are not described in section 4 of the generic specification.

Each detail specification shall prescribe all tests and measurement procedures required for lot-by-lot inspection and periodic testing. It shall, as a minimum, include the relevant tests given in this specification with stated methods and severities.